Amendments to the claims:

This listing of claims will replace all prior versions and listings of claims in this application:

1. (Original) 1. A turbo decoder comprising a plurality of component decoders for decoding component code words of turbo codes, each component decoder comprising: circuits for receiving and storing received symbols corresponding to a turbo code word; a gamma block for calculating substantially simultaneously for a plurality of decoder trellis stages a plurality of first and second gamma probability function values, which correspond to the branches of a component code's trellis, the gamma block receiving as inputs the received symbols' channel transition probabilities and a priori bit probabilities for the bits represented by the received symbols, which correspond to the decoder trellis stages; an alpha block for receiving the gamma probability function values from the gamma block and for recursively calculating alpha probability function values, corresponding to a plurality of trellis state indices, substantially simultaneously by a plurality of circuits, the gamma function values for each alpha probability function value being selected via selection switches, the alpha block further receiving a plurality of alpha probability function values from the previous step of the recursive calculation, the alpha block further comprising circuits for scaling each resultant alpha probability function value substantially simultaneously by a scale factor which is provided as an input to the alpha block; a beta block for receiving first gamma probability function values from the gamma block and for recursively calculating beta probability function values, corresponding to a plurality of trellis state indices, substantially simultaneously by a plurality of circuits, the gamma function values for each beta probability function value being selected via selection switches, the beta block further receiving a plurality of beta probability function values from the previous step of the recursive calculation, the beta block signal processing further comprising circuits to scale each resultant beta probability function value substantially simultaneously by a scale factor which is provided as an input to the beta block; a sigma block for receiving the alpha and beta probability function values, respectively, from the alpha and beta blocks, respectively, receiving the second gamma probability function values from the gamma block and receiving a second set of alpha and beta probability function values, respectively, from alpha and beta memories, respectively, and for calculating substantially simultaneously for a plurality of decoder trellis stages a plurality of sigma probability function values which correspond to the branches of a component code's trellis at the trellis stages corresponding to the received symbols, which are being processed at that time, the sigma block also comprising a plurality of pipelined trees of summation functions of all sigma values belonging to each of two subsets of the sigma probability function values for each of the plurality of decoder trellis stages, one subset comprising the sigma function values for trellis branches labeled with a data bit value of zero and the other subset comprising the sigma function values for trellis branches labeled with a data bit value of one, the sigma block calculating the difference of the outputs of the two summation functions for each of the plurality of decoder trellis stages to produce the logarithm of the likelihood ratio of the maximum a posteriori decoded bit value probabilities for each of the plurality of trellis stages as outputs of the turbo decoder; a plurality of memory cells for storing

channel transition probabilities, received symbols, half of the alpha probability function values, half of the beta probability function values, a posteriori and a priori data bit log-likelihood ratios, and a de- interleaving pattern; a circuit for calculating the negative of the logarithm of the probability that a decoded data bit value is zero from the log-likelihood ratio of data bit value probabilities; a circuit for calculating the negative of the logarithm of the probability that a decoded data bit value is one from the log-likelihood ratio of data bit value probabilities; a circuit for making decoded bit decisions from the corresponding log-likelihood ratio; and a circuit for outputting decoded data bits.

2. (New) A turbo decoder comprising:

a gamma block for providing posteriori state probability estimates;

an alpha block for recursively calculating alpha probability function values; and

a beta block for recursively calculating beta probability function values, wherein said gamma block provides gamma probability estimates to at least one of said alpha and beta blocks for calculating at least one of said alpha and beta probability function values substantially simultaneously.

3. (New) A turbo decoder in accordance with claim 2, wherein said gamma probability estimates are provided to at least one of said alpha and beta blocks via selection switches to perform at least one of said alpha or beta recursions in parallel.

4. (New) A turbo decoder in accordance with claim 2, further comprising a normalization circuit that monitors the alpha and beta probability function values and prescribes a scale factor to at least one of said function values such that all such function values at a trellis level remain within certain limits.

5. (New) A turbo decoder in accordance with claim 4, wherein previously calculated values of the alpha and beta probability functions are used within the normalization circuit in order to remove a normalization calculation from the alpha block and the beta block to increase decoding speed.

6. (New) A turbo decoder in accordance with claim 2, wherein the alpha and beta probability function values are provided to a sigma block to determine a posteriori state transition probability estimates and generate soft-decision outputs.

7. (New) A turbo decoder in accordance with claim 2, wherein said gamma block further comprises a gamma calculator circuit for computing gamma values.

8. (New) A turbo decoder in accordance with claim 7, wherein said gamma calculator circuit computes four gamma probabilities at each trellis level for a rate half-component code.

9. (New) A turbo decoder in accordance with claim 7, wherein said gamma probabilities are represented by the following expressions:

$$\gamma_{t,00}(m',m) = \mathrm{AP_t}(0) \bullet \mathrm{R}(Y_{t_i} \mid 0) \bullet R(Y_{t_p} \mid 0)$$
$$\gamma_{t,01}(m',m) = \mathrm{AP_t}(0) \bullet \mathrm{R}(Y_{t_i} \mid 0) \bullet R(Y_{t_p} \mid 1)$$
$$\gamma_{t,10}(m',m) = \mathrm{AP_t}(1) \bullet \mathrm{R}(Y_{t_i} \mid 1) \bullet R(Y_{t_p} \mid 0)$$
$$\gamma_{t,11}(m',m) = \mathrm{AP_t}(1) \bullet \mathrm{R}(Y_{t_i} \mid 1) \bullet R(Y_{t_p} \mid 1)$$

where $\mathrm{AP_t}$ is the a priori probability for a systematic bit at trellis level $_t$; and $\mathrm{R}Y_{t_i}$ and RY_{t_p} are channel transition probabilities.

10. (New) A turbo decoder in accordance with claim 9, wherein said gamma calculator includes a look-up table to calculate each channel transition probability function $\mathrm{R}(\bullet|\bullet)$.

11. (New) A turbo decoder in accordance with claim 9, wherein said gamma calculator includes a look-up table containing the values R(y|1) and R(y|0) for only either y>0.5 or y<0.5.

12. (New) A turbo decoder in accordance with claim 11, wherein said gamma calculator includes a look-up table that is scaled such that for each value of y, one of the values R(y|1) or R(y|0) is exactly unity.

13. (New) A decoder comprising:

a decoding algorithm that computes alpha probabilities, wherein each of said alpha probabilities corresponding to a single trellis level are computed in parallel.

14. (New) A decoder comprising:

a decoding algorithm that includes a circuit for computing four gamma probabilities at each trellis level for a rate half-component code.

15. (New) A decoder comprising:

a decoding algorithm that computes beta probabilities, wherein each of said beta probabilities corresponding to a trellis level are computed in parallel.

16. (New) A decoder comprising:

a decoding algorithm that computes alpha probabilities and a single normalization value and applies said normalization value to all alpha probabilities at a trellis level in parallel.

17. (New) A decoder comprising:

a decoding algorithm that computes sigma probabilities, wherein each of said sigma probabilities corresponding to a trellis level are computed in parallel.

18. (New) A decoder comprising:

a decoding algorithm that computes alpha probabilities in a direction R and simultaneously computes beta probabilities in a direction L, wherein each of said probabilities corresponds to a single trellis level, wherein said decoding algorithm stores each respective probability set until L equals R, after L equals R said decoding algorithm continues to calculate alpha probabilities and beta probabilities in real time while simultaneously reading previously stored alpha and beta probability sets.

19. (New) A decoder in accordance with claim 18, wherein said decoding algorithm further computes two sets of sigma probabilities, a first set using a real time alpha probability set with a stored beta probability set and a second set using a real time beta probability set with a stored alpha probability set.

20. (New) A decoder in accordance with claim 18, wherein the sigma probabilities within a respective sigma probability set associated with the same data value are used to determine the probability of that data value.

21. (New) A decoder comprising:

a decoding algorithm that computes at least one of alpha or beta probabilities, wherein said at least one of said alpha or beta probabilities are computed according to an update rule that includes a normalization factor.

22. (New) A decoder in accordance with claim 21, wherein said normalization factor is computed as a function of a probability set from a previous trellis level.

23. (New) A decoder in accordance with claim 22, wherein said normalization factor is computesd as the maximum of a probability set from a previous trellis level.

24. (New) A circuit for calculating the alpha or beta update recursion in a MAP decoder, wherein said circuit contains selection switches that select two gamma probabilities from a set of input gamma probabilities, wherein an output from said selection switches is combined with at least one of two alpha probabilities or two beta probabilities.

25. (New) A circuit in accordance with claim 24, further comprising multiplexers to select the routing of said alpha or said beta probabilities and enabling a code generator to be programmable.

26. (New) A decoder comprising:

a circuit for calculating at least one of an alpha or beta update recursion in a log-MAP decoder, wherein said circuit implements a log-domain addition using two parallel branches, wherein one of said branches performs a select-largest-value function and the second of said branches computes a correction value dependent on a difference of two values.

27. (New) A decoder in accordance with claim 26, wherein the second of said branches computes the correction value using a look-up table implemented as at least one of ROM, RAM or combinatorial logic.

28. (New) A decoder in accordance with claim 27, wherein the contents of said lookup table are manipulated such that the operation following said lookup table is implemented using positive integer arithmetic.

STATEMENT UNDER RULE 37 CFR 1.173(c)

In accordance with the provisions of 37 CFR 1.173(c), the following remarks are made with respect to the status of and support for the newly added claims 2-28.

Claims 1-28 are currently pending. New claims 2-28 have been added. No claims have been canceled.

New claims 2-28 have been added to claim inventive material originally disclosed within the instant application but not covered by original claim 1. The Applicants had claimed less than they had a right to claim and have filed this reissue application to correct this error, which error was made without any deceptive intent. Each new claim as presented in this reissue application is described in the original patent specification and enabled by the original patent specification such that 35 USC §112 is satisfied. Nothing in the original patent specification indicates an intent not to claim the subject matter of the claims presented in the reissue application. The original patent also evidences that the Applicants intended to claim the material or that the Applicants considered the material now claimed to be inventive material. In this regard, see for example Column 1, Lines 37-42, "*It is desirable to provide a turbo decoder which efficiently uses memory and combinatorial logic such that the structure thereof is highly streamlined with parallel signal processing. It is further desirable to provide such a structure which is amenable to implementation on an application specific integrated circuit (ASIC).*"

The Applicant will now discuss each new claim:

New claim 2 recites a turbo decoder comprising: a gamma block for providing posteriori state probability estimates; an alpha block for recursively calculating alpha probability function values; and a beta block for recursively calculating beta probability function values, wherein the gamma block provides gamma probability estimates to at least one of the alpha and beta blocks for calculating at least one of the alpha and beta probability function values substantially simultaneously. This claim is fully supported in the specification. See for example, Column 1, Lines 45-58, Column 7, lines 1-7 and Figure 6.

New claim 3 recites a turbo decoder in accordance with claim 2, wherein the gamma probability estimates are provided to at least one of said alpha and beta blocks via selection switches to perform at least one of said alpha or beta recursions in parallel. This claim is fully supported in the specification. See for example, Column 1, Lines 53-58, Column 4, lines 36-40, and Column 7, Lines 36-49.

New claim 4 recites a turbo decoder in accordance with claim 2, further comprising a normalization circuit that monitors the alpha and beta probability function values and prescribes a scale factor to at least one of the function values such that all such function values at a trellis level remain within certain limits. This claim is fully supported in the

specification. See for example, Column 1, Lines 60-63, Column 7, lines 50-58, Column 13, Lines 9-67 and Column 14, Lines 1-62.

New claim 5 recites a turbo decoder in accordance with claim 4, wherein previously calculated values of the alpha and beta probability functions are used within the normalization circuit in order to remove a normalization calculation from the alpha block and the beta block to increase decoding speed. This claim is fully supported in the specification. See for example, Column 1, Lines 63-67, Column 7, Lines 50-67, and Column 8, Lines 1-16.

New claim 6 recites a turbo decoder in accordance with claim 2, wherein the alpha and beta probability function values are provided to a sigma block to determine a posteriori state transition probability estimates and generate soft-decision outputs. This claim is fully supported in the specification. See for example, Column 1, Line 67, Column 2, Lines 1-5, and Column 8, Lines 17-45.

New claim 7 recites a turbo decoder in accordance with claim 2, wherein the gamma block further comprises a gamma calculator circuit for computing gamma values. This claim is fully supported in the specification. See for example, Column 5, Line 54-55 and Column 8, Lines 46-52.

New claim 8 recites a turbo decoder in accordance with claim 7, wherein the gamma calculator circuit computes four gamma probabilities at each trellis level for a rate half-component code. This claim is fully supported in the specification. See for example, Column 5, Lines 30-60.

New claim 9 recites a turbo decoder in accordance with claim 7, wherein the gamma probabilities are represented by the following expressions:

$$\gamma_{t,00}(m',m) = \mathrm{AP_t}(0) \bullet \mathrm{R}(Y_{t_i} \mid 0) \bullet R(Y_{t_p} \mid 0)$$
$$\gamma_{t,01}(m',m) = \mathrm{AP_t}(0) \bullet \mathrm{R}(Y_{t_i} \mid 0) \bullet R(Y_{t_p} \mid 1)$$
$$\gamma_{t,10}(m',m) = \mathrm{AP_t}(1) \bullet \mathrm{R}(Y_{t_i} \mid 1) \bullet R(Y_{t_p} \mid 0)$$
$$\gamma_{t,11}(m',m) = \mathrm{AP_t}(1) \bullet \mathrm{R}(Y_{t_i} \mid 1) \bullet R(Y_{t_p} \mid 1)$$

where $\mathrm{AP_t}$ is the a priori probability for a systematic bit at trellis level $_t$; and $\mathrm{R}Y_{t_i}$ and RY_{t_p} are channel transition probabilities. This claim is fully supported in the specification. See for example, Column 5, Lines 35-40.

New claim 10 recites a turbo decoder in accordance with claim 9, wherein the gamma calculator includes a look-up table to calculate each channel transition probability function $\mathrm{R}(\bullet|\bullet)$. This claim is fully supported in the specification. See for example, Column 5, Lines 62-67.

New claim 11 recites a turbo decoder in accordance with claim 9, wherein the gamma calculator includes a look-up table containing the values R(y|1) and R(y|0) for only either y>0.5 or y<0.5. This claim is fully supported in the specification. See for example, Column 6, Lines 7-22.

New claim 12 recites a turbo decoder in accordance with claim 11, wherein the gamma calculator includes a look-up table that is scaled such that for each value of y, one of the values R(y|1) or R(y|0) is exactly unity. This claim is fully supported in the specification. See for example, Column 6, Lines 23-35.

New claim 13 recites a decoder comprising a decoding algorithm that computes alpha probabilities, wherein each of said alpha probabilities corresponding to a single trellis level are computed in parallel. This claim is fully supported in the specification. See for example, Column 7, Lines 1-7 and Figure 3.

New claim 14 recites a decoder comprising a decoding algorithm that includes a circuit for computing four gamma probabilities at each trellis level for a rate half-component code. This claim is fully supported in the specification. See for example, Column 5, Lines 30-60 and Figure 2.

New claim 15 recites a decoder comprising a decoding algorithm that computes beta probabilities, wherein each of said beta probabilities corresponding to a trellis level are computed in parallel. This claim is fully supported in the specification. See for example, Column 7, Lines 1-7 and Figure 3.

New claim 16 recites a decoder comprising a decoding algorithm that computes alpha probabilities and a single normalization value and applies said normalization value to all alpha probabilities at a trellis level in parallel. This claim is fully supported in the specification. See for example, Column 1, Lines 60-63 and Figure 3 and Column 13, Lines 8-67 and Column 14, Lines 1-6)

New claim 17 recites a decoder comprising a decoding algorithm that computes sigma probabilities, wherein each of said sigma probabilities corresponding to a trellis level are computed in parallel. This claim is fully supported in the specification. See for example, Column 10, Lines 4-15.

New claim 18 recites a decoder comprising a decoding algorithm that computes alpha probabilities in a direction R and simultaneously computes beta probabilities in a direction L, wherein each of said probabilities corresponds to a single trellis level, wherein said decoding algorithm stores each respective probability set until L equals R, after L equals R said decoding algorithm continues to calculate alpha probabilities and beta probabilities in real time while simultaneously reading previously stored alpha and beta probability sets. This claim is fully supported in the specification. See for example, FIG 5a and Paragraph 8, Lines 28-45.

New claim 19 recites a decoder in accordance with claim 18, wherein the decoding algorithm further computes two sets of sigma probabilities, a first set using a real time alpha probability set with a stored beta probability set and a second set using a real time beta probability set with a stored alpha probability set. This claim is fully supported in the specification. See for example, FIG 5a and Column 8, Lines 28-45.

New claim 20 recites a decoder in accordance with claim 18, wherein the sigma probabilities within a respective sigma probability set associated with the same data value are used to determine the probability of that data value. This claim is fully supported in the specification. See for example, Column 8, Lines 28-45.

New claim 21 recites a decoder comprising a decoding algorithm that computes at least one of alpha or beta probabilities, wherein at least one of the alpha or beta probabilities is computed according to an update rule that includes a normalization factor. This claim is fully supported in the specification. See for example, Column 10, Lines 21-27.

New claim 22 recites a decoder in accordance with claim 21, wherein the normalization factor is computed as a function of a probability set from a previous trellis level. This claim is fully supported in the specification. See for example, Column 10, Lines 21-27.

New claim 23 recites a decoder in accordance with claim 22, wherein the normalization factor is computesd as the maximum of a probability set from a previous trellis level. This claim is fully supported in the specification. See for example, Column 14, Lines 55-60.

New claim 24 recites a circuit for calculating the alpha or beta update recursion in a MAP decoder, wherein the circuit contains selection switches that select two gamma probabilities from a set of input gamma probabilities, wherein an output from the selection switches is combined with at least one of two alpha probabilities or two beta probabilities. This claim is fully supported in the specification. See for example, Column 10, Lines 11-12 and Column 12, Lines 17-18.

New claim 25 recites a circuit in accordance with claim 24, further comprising multiplexers to select the routing of the alpha or beta probabilities and enabling a code generator to be programmable. This claim is fully supported in the specification. See for example, Column 11, Lines 14-15 and Column 12, Lines 17-21.

New claim 26 recites a decoder comprising a circuit for calculating at least one of an alpha or beta update recursion in a log-MAP decoder, wherein the circuit implements a log-domain addition using two parallel branches, wherein one of the branches performs a select-largest-value function and the second of the branches computes a correction value dependent on a difference of two values. This claim is fully supported in the specification. See for example, Column 10, Lines 63-66 and Column 11, Lines 11-16.

New claim 27 recites a decoder in accordance with claim 26, wherein the second of the branches computes the correction value using a look-up table implemented as at least one of ROM, RAM or combinatorial logic. This claim is fully supported in the specification. See for example, Column 11, Lines 11-16 and Column 11, Lines 55-65.

New claim 28 recites a decoder in accordance with claim 27, wherein the contents of the lookup table are manipulated such that the operation following said lookup table is implemented using positive integer arithmetic. This claim is fully supported in the specification. See for example, Column 11, Lines 40-54.

In view of the foregoing amendments and remarks, it is respectfully submitted that claims 1-28 are allowable. An early and favorable action on this application is respectfully requested.

Should the Examiner believe that any further action is necessary in order to place this application in even better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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